Abstract of the Disclosure

An equalizer for return-to-zero (RZ) signals comprises: (a) an equalizer core for equalizing the received signal; (b) a decision corrector for detecting and correcting misplaced pulses and double pulses in the equalized signal using known characteristics and properties of the RZ signal itself; and (c) an error calculator that generates an error signal for updating tap values based on the initial outputs of the equalizer core and the corrected outputs of the decision corrector. The decision corrector comprises a zero assertion counter that generates a clock synchronized with the timing of the received signal, and corrects the equalized signal by forcing zeroes in those portions of the equalized signal that the synchronized clock indicates should be "RZ" zeroes (as opposed to "data" zeroes or "data" symbols "1" or "-1"). The decision corrector further comprises a misplaced pulse detector for detecting misplaced pulses and double pulses based on both the output of the zero assertion counter and coding in the RZ signal, and corrects the equalized signal by moving the misplaced pulse or doubled portion of the pulse forward or backward in time in accordance with the principles of the RZ coding scheme used. The equalizer can further comprise interpolators for generating a plurality of signals based on the equalized signal, to provide a greater diversity of information for the decision corrector.